[*COLLAPSIBLE PIPELINE STRUCTURE AND METHOD USED IN A MICROPROCESSOR*]

Abstract of Disclosure

A collapsible pipeline structure, suitable for use in a microprocessor. The contains a first pipeline stage, under control by a clock to export a sequence of instruction stage results with respect to a clock cycle of the clock. A bypassing storage unit receives the sequence of instruction stage results and, when operating in collapsed mode, forwards that sequence onto the subsequent pipeline stage, bypassing the storage unit through a mutiplexer. A second pipeline stage receives the output from the bypassing storage unit, and exports its instruction stage results under control of the clock. Wherein if the collapsing function of the bypassing storage unit is disabled, then the instruction pipeline functions in the conventional manner.

Figures